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EXAMINER	
DINH, TUAN T	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Application Number: 10/056,270
Filing Date: January 24, 2002
Appellant(s): KUCHARSKI, JANUSZ M.

Jon M. Powers
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/25/07 appealing from the Office action mailed 09/20/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal: Appellant's discussion of related appeals and interferences is accurated.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

U.S. Patent 6,353,540	Akiba et al.	03-2002
U.S. Patent 4,904,968	Theus	02-1990
JP 406069680A	Hirashiro et al.	03-1994

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiba et al. (U.S. Patent 6,353,540) in view of Theus (U.S. Patent 4,904,968).

As to claim 1, Akiba et al. discloses an electronic device as shown in figures 33-34 comprising:

a circuit board (23, figure 34-column 18, line 33);

a first circuit (26, column 18, lines 50-51) disposed on a first side (a top side) of the circuit board, the first circuit connected to a first ground plane (15, column 18, line 52) of the circuit board;

a second circuit (28, column 18, line 61) disposed on a second side (a bottom side) of the circuit board, wherein the second side is opposite the first side, the second circuit connected to a second ground plane (21, column 18, line 63) of the circuit board; and

wherein the first and second ground planes (15, 21) respectively lie in different planes (see figure 34) of the circuit board (23) and are electrically interconnected by a conductive trace (figure 34 shows a circuitry electrically connected the first and second grounds 15, 21 through a resistor Rc) disposed within the circuit board.

Akiba et al. specific does not disclose the second circuit operating at current levels substantially lower than the first circuit.

Theus shows a circuit board (10, column 4, line 62) comprising a first circuit (58) connected to a first ground plane (70), and a second circuit (12) connected to a second ground (36), the first and second ground planes are formed in a different plane, see figure 4, the second circuit (12) operating at current levels substantially lower than the first circuit (see abstract, and column 4, lines 39-42).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the circuit board having the second circuit operating at current levels substantially lower than the first circuit as taught by Theus employed in the device of Akiba et al in order to provide a radiation of the unnecessary electromagnetic wave due to the voltage variation between a power source and ground.

As to claims 2-4, Akiba et al. discloses the first circuit (26), which is a switch mode power supply, a forward-type switch mode power supply, or a flyback-type switch mode power supply, see figure 34, column 18, lines 50-51.

As to claim 6, Akiba et al. discloses the first circuit being adapted to power the second circuit.

As to claims 11-13, Akiba et al. discloses the device as shown in figure 1the circuit board comprises two or more layers (column 18, line 33) disposed between the first and second sides, and the first ground plane (15) is disposed on one of the two or more layers (S1, V1, and S2) and the second ground plane (21) is disposed on another of the two or more layers (S3, V2, and S4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 16-17, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiba et al. ('540) in view of Theus ('968), and further in view of Hirashiro et al. (JP 406069680A, hereafter JP).

As to claims 5, and 16-17, Akiba and Theus disclose all of the limitations of the claimed invention, see claim 1, except for the second circuit being a control circuit controlling the first circuit. JP shows a second circuit that controls a first circuit.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a second circuit controls a first circuit, as taught by JP, employed in the printed circuit board of Akiba and Theus in order to facilitate control voltage to a power supply of a circuit board.

As to claims 22-24, Akiba et al. discloses the device as shown in figure 1the circuit board comprises two or more layers (column 18, line 33) disposed between the first and second sides, and the first ground plane (15) is disposed on one of the two or more layers (S1, V1, and S2) and the second ground plane (21) is disposed on another of the two or more layers (S3, V2, and S4).

(10) Response to Argument

Appellant argues:

a) Akiba et al. does not disclose "a conductive trace disposed within the circuit board."

b) "Nowhere does Akiba et al. teach or suggest that the resistor Rc of Figure 34 is a trace or Akiba is silent as to having the resistor Rc disposed within the circuit board."

c) The combination of Akiba and Theus do not teach "the second circuit operates at current levels substantially lower than the first circuit."

A conductive path on top of a PCB made of copper. The copper trace is embedded on the surface of a PCB and forms a circuit when electronic components are soldered to it.

Examiner disagrees.

Response to arguments (a) and (b):

First, the conductive trace is well defined as a conductive path, wiring, or pattern on top or embedded in a printed circuit board (PCB) and forms a circuit (or a circuit line) when electronic components are soldered to it. Also, the conductive trace can be used as signal, power, or ground traces.

Akiba discloses in figure 34 that shows a conductive trace or circuitry forming a conductive path electrically connected the first and second grounds 15, 21 together through a resistor Rc. The conductive path is formed and disposed (embedded) within the circuit board (23).

Second, in the Office action, the examiner does not mention the resistor (Rc) formed as the conductive trace, but the resistor (Rc) is electrically connected to the conductive trace/path to form the rectangular path of between the two ground planes (15 and 21).

So, the examiner believes the rejection is proper and read on all of limitations of the claimed invention.

Response to arguments (c):

Akiba discloses the two circuit devices (26, 28) connected to the two different ground planes (G15, G21), and because the devices 26,and 28 are different so that when they are connected to the ground planes then they are (the device 26 and 28) capable of being operated at different current levels, even though the reference does not specific express discloses, but that is well known skill in the art that the disclosed

devices (components) electrically connected through the ground planes that performed the different current levels (**noted**: the examiner did discuss with Mr. Fogg on the interview on 05/12/06 on the Akiba reference), and further for the applicant benefit, Theus teaches two components (50 and 12) electrically connected to different ground planes (70 and 36) and operated at different current levels.

So, the examiner believes the rejection is proper and read on all of limitations of the claimed invention.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

TUAN T. DINH
PRIMARY EXAMINER

Tuan Dinh 9/17/09.

September 05, 2007.

Conferees:

(SPE) Darren Schuberg.

(SPE) Dean Reichard.